Global AI Trend Tracker

Global Markets Research
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EQUITY: TECHNOLOGY

Google's next-gen AI network for TPUv8t / v8i...

...And implications for the AI networking value chain

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TPU v8t & v8i's networking architecture may lead to stronger demand for OCS and benefit Google's TPU supply chain

Google (GOOG US, Not rated) released its eighth-generation tensor processing unit (TPU) at its Cloud Next 2026 in April, and the company for the first time distinguished its TPU products into training (TPU 8t) and inference (TPU vi). TPU 8t improves large-scale pre-training performance with SparseCore cores and Virgo network topology, while TPU 8i is designed for real-time reasoning and complex decision-making, with CAE (Collectives Acceleration Engine) and new Boardfly topology solving the latency bottleneck of long context reasoning to a certain extent. We think the purpose-built networks for TPUv8t and v8i reflect the AI market trend of decoupling network architecture for training and inference, in order to better unlock their performance in different scenarios, while reducing cost and power consumption at the same time. We think **Boardfly network brings incremental demand for optical circuit switches (OCS0 at both the scale-up and the scale-out level)**. Meanwhile, as a technology leader in optical networks, we expect Google's stronger TPU shipments of would accelerate its adoption of all the mainstream optical communication solutions, including **1.6T pluggable transceivers, NPO (near-field packaged optics) and CPO (co-packaged optics)**. We think this is **positive for Google's TPU supply chain, including substrate and PCB suppliers such as VGT (300476 CH/2476 HK, Buy), as well as optical communication solution providers**.

Google introduced Virgo Network and Boardfly topology for TPU 8t and 8i, respectively, aiming at lower latency and higher bandwidth

Regarding networking solutions, TPU 8t still uses 3D Torus topology (similar to TPU v7) to connect chips at the scale-up level to form a pod with up to 9,600 cards, and we think that there are still 48 OCS in each pod, but the number of ports may increase to 300*300 (from 288*288). Google introduced Virgo Network, a flat two-layer non-blocking topology, for TPU V8t scale-out network. According to the company, this new network architecture enables up to 4x increased data center network (DCN) bandwidth and uses high-radix switches that reduce network layers by allowing more ports per switch. Moreover, Google has designed a new network topology, called Boardfly, for the TPU 8i cluster that can connect up to 1,152 of chips. The network connects 8 boards via copper cabling and further scales to 36 groups (up to 1,024 active chips) linked through OCS.

Growth of CPU demand accelerates in agentic era

In addition, both eighth-generation TPU chips will be working with Google's self-developed ARM-based Axion CPU as the main controller. We think CPUs may become the key to running large AI clusters in the future, due to the exponential growth of inference workloads. According to comments from Intel's CEO during the company's 1Q26 earnings call, the CPU-to-GPU attach rate used to be 1:8, which has increased to 1:4 now, and may increase to 1:1 in the future. We think this reflects growing demand for CPUs in AI clusters for the agentic era.

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Introduction to TPU V8i & V8t

On 22 April 2026, Google released its eighth-generation TPU at the Cloud Next 2026 conference, which is divided into the TPU 8t training chip and the TPU 8i inference chip. From the perspective of Google's chip development path, the current divergence between training and inference architecture requirements is widening, with training clusters focusing on optimizing computing power and inference clusters focusing on optimizing HBM bandwidth and memory capacity. The current mainstream large language models (LLM) are all MoE architectures, which require long context reasoning and the chain of thought scheme, and the importance of communication efficiency, memory access speed, and low-latency synchronization between chips far exceeds that of single-chip computing power. Therefore, Google designed the training chip and the inference chip separately and optimized their internal architectures to achieve high computing performance and low latency for the training chip, and high memory and low power consumption for the inference chip.

Fig. 1: Development path of Google TPU

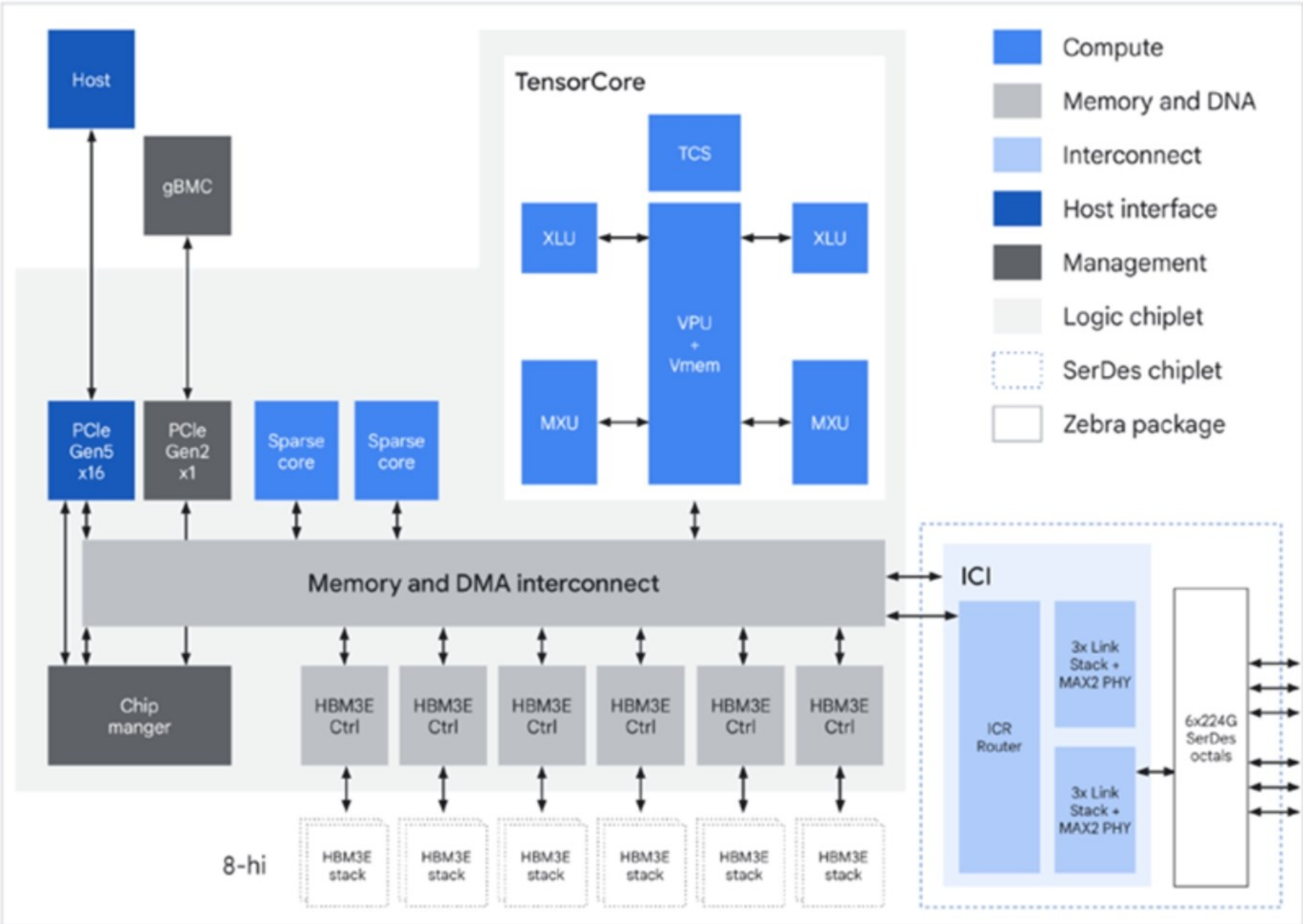
	TPU	TPU chips per superpod	Topology	ICI bandwidth per TPU chip	ICI optical transceiver	Optical lane rate	OCS
2018	v2	256	2D Torus	800GB/s	None	NA	None
2020	v3	1024	2D Torus	800GB/s	400G AOC	50G	None
2022	v4	4096	3D Torus	600GB/s	400G OSFP	50G	OCS
2023	v5p	8960	3D Torus	1200GB/s	800G OSFP	100G	OCS
2025	v7	9216	3D Torus	1200GB/s	800G OSFP	200G	OCS
2026	V8t	9600	3D Torus	2400GB/s	NA	400G	OCS
2026	V8i	1152	Boardfly	2400GB/s	NA	400G	OCS

Source: Google, Nomura research

TPU 8t improves large-scale pre-training performance with SparseCore and Virgo network topology. TPU 8i is designed for real-time reasoning and complex decision-making, and its CAE acceleration engine and new Boardfly topology solve the latency bottleneck of long context reasoning to a certain extent, allowing AI to evolve from single-next-word prediction to scene simulation and deep logical reasoning, and AI responses will become more timely and coherent. Supported by the computing power of Google's self-developed ARM Axion architecture CPUs, Boardfly topology has achieved a double leap in energy efficiency.

The SparseCore is a specialized accelerator designed to handle the irregular memory access patterns of embedding lookups. The MoE LLM only activates a small number of parameters each time, and although the hybrid expert technology is highly energy efficient, it produces a large number of irregular memory accesses. SparseCore technology is specifically designed to handle this task, working with the Matrix Multiply Unit (MXU) to keep the chip running at high load. Moreover, TPU 8t minimizes exposed vector operation time by implementing more balanced Vector Processing Unit (VPU) scaling. In terms of computing, TPU 8t introduces native 4-bit floating point (FP4) to overcome memory bandwidth bottlenecks, doubling MXU throughput while maintaining accuracy for LLMs even at lower-precision quantization. In terms of memory, TPU 8t adopts de-intermediated TPU Direct technology, and HBM memory can directly talk to the Network Interface Card (NIC), bypassing the CPU and DRAM, resulting in 10x faster memory access speed than the previous generation TPU. Overall, TPU 8t solves several key bottlenecks in training tasks: efficiently processing sparse data, reducing data handling overhead between memory and compute units, and optimizing network communication between large-scale chip clusters. Google claims that compared with the previous generation, the "performance per dollar" of the 8T in training scenarios can be improved by up to 2.7x.

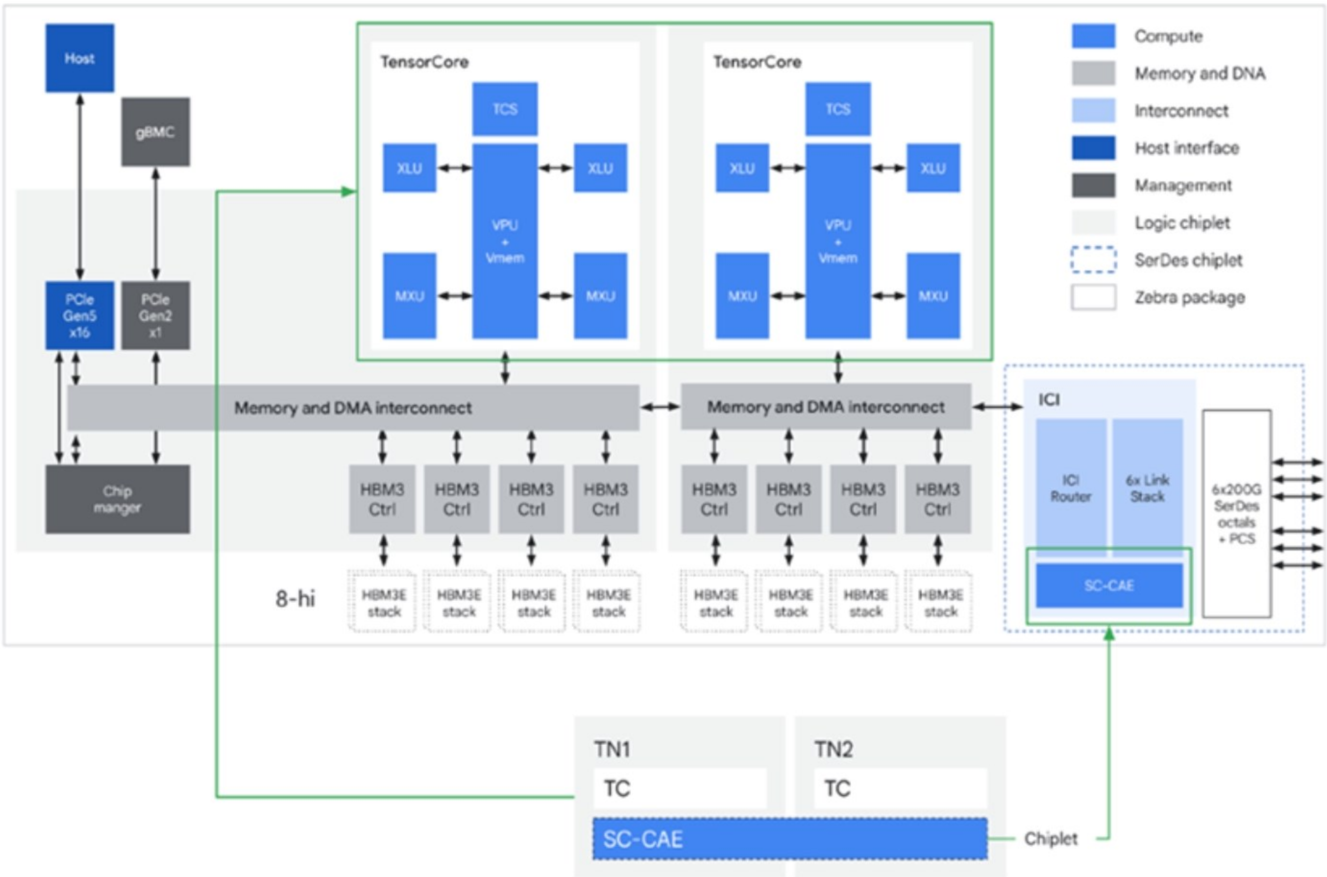
Fig. 2: TPU 8t ASIC block diagram



Source: Google, Nomura research

TPU 8i is a new chip designed for inference tasks, with the most notable feature being the tilt of resource allocation towards memory. Although its peak hash rate is lower than that of 8t, it is equipped with a 384MB on-chip SRAM cache (3x that of 8t), higher HBM memory capacity (288GB), and greater bandwidth. Google claimed that TPU 8i can host a larger KV Cache entirely on silicon, significantly reducing the idle time of the cores during long-context decoding. In addition, when an LLM performs inference, chips need to frequently synchronize data and summarize results, a process called collective communication. Chains-of-thought require multiple computing cores to frequently synchronize intermediate results, and traditional synchronization operations have extremely high latency. Therefore, TPU 8i uses the CAE, which aggregates results across cores with near-zero latency, specifically accelerating the reduction and synchronization steps required during auto-regressive decoding and chain-of-thought processing. For each TPU 8i chip, there are two Tensor Cores (TC) on-core dies and one CAE on the chiplet die, replacing four SparseCores (SCs) on core dies in the previous-generation Ironwood TPU. CAE further reduces the on-chip latency of collectives by 5x. Lower latency per collective operation means less time spent waiting, directly contributing to higher throughput required to run millions of agents concurrently.

Fig. 3: TPU 8i ASIC block diagram



Source: Google, Nomura research

Fig. 4: Comparison of TPU v7, TPU v8t and TPU v8i

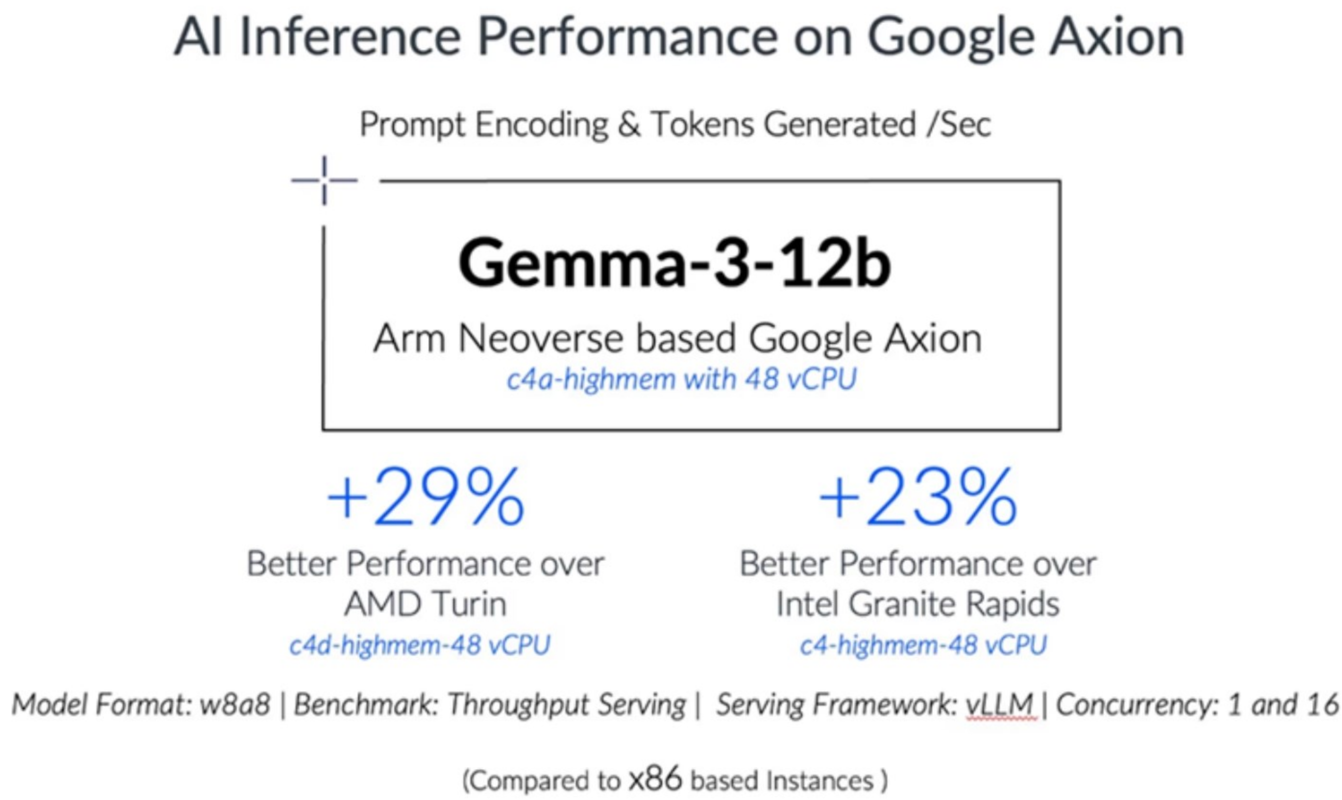
	TPU v7	TPU 8t	TPU 8i
Primary workload	High-performance ASIC for training and inference	Focus on large-scale training	Focus on large-scale inference
Design of die	Dual die	Single die	Dual die
HBM capacity	192GB HBM3E	216GB HBM	288GB HBM
HBM bandwidth	7.3TB/s	6.5TB/s	8.6TB/s
on-chip SRAM	-	128MB	384MB
Core feature	SparseCore, shared memory	SparseCore and LLM decoder engine, native FP4, Vrigo network	CAE, large SRAM, Boardfly network
Pod size	9216	9600	1152
Network topology	3D Torus	3D Torus	Boardfly
Peak FP4 PFLOPs	4.6	12.6	10.1

Source: Google, Nomura research

With the explosive growth of inference workloads, CPUs are the key to determining the efficiency and cost of AI systems. Data orchestration and memory management of inference tasks are highly dependent on the CPU, and the "logical scheduling" and "serial processing" used by AI Agents to perform complex tasks such as reading databases, running code, and parsing documents are the expertise of CPUs. According to comments from the Intel CEO during the company's 1Q26 earnings call, the CPU-to-GPU attach rate used to be 1:8, which has increased to 1:4 now, and may increase to 1:1 in the future. We think this reflects growing demand for CPU in AI clusters for agentic era.

Axion is Google's first custom ARM architecture-based CPU designed specifically for data centers, announced in 2024. For AI inference, Axion's dedicated optimizations can significantly boost performance, enabling AI workloads to run faster and more efficiently, according to management. The Axion product portfolio now includes three options: N4A, C4A, and C4A metal. Compared to virtual machines using mainstream x86 architecture CPUs, N4A offers twice the cost-performance ratio and leads in energy efficiency by up to 80% per watt, according to Google. In the TPU v8 series, Google is the first to use the Axion CPU as the main computing header, effectively reducing data preprocessing latency and ensuring the TPU computing engine runs at full capacity.

Fig. 5: AI inference performance on Axion CPU

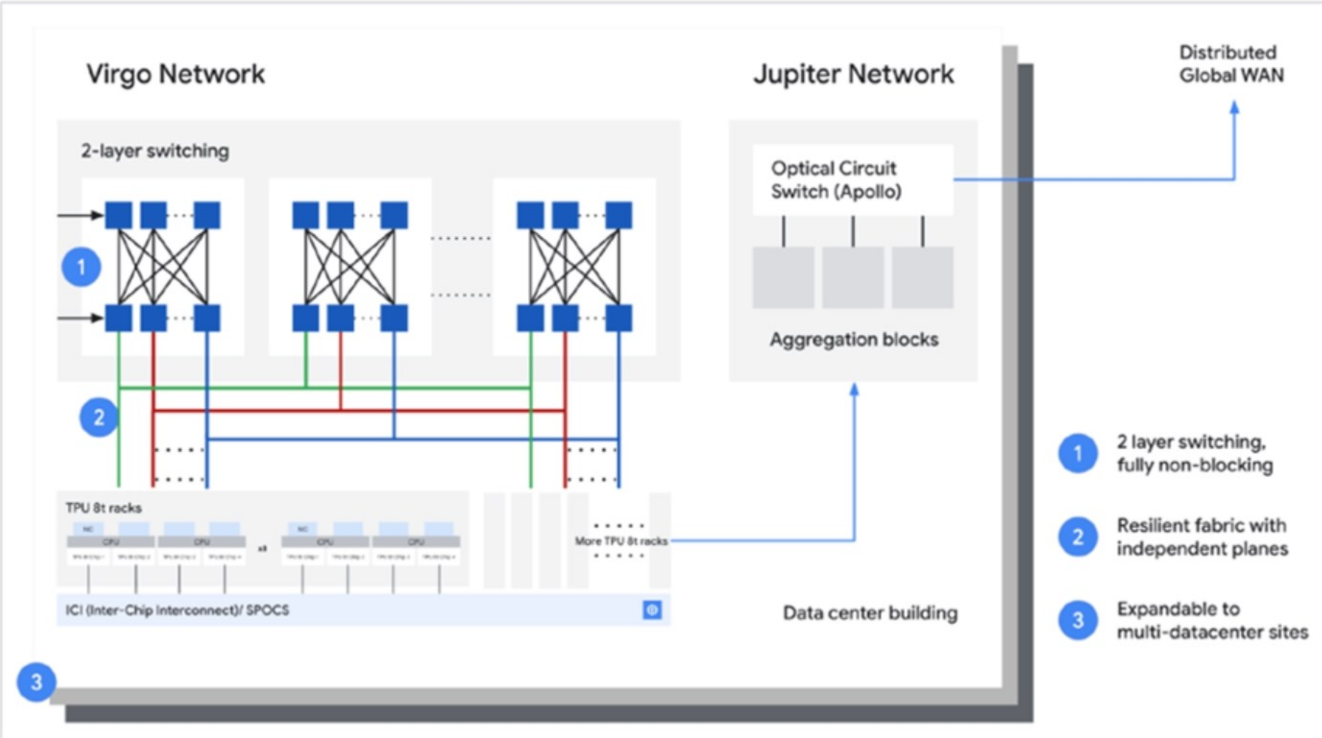


Source: Google, Nomura research

TPU V8i & V8t networking solutions

TPU 8t still uses 3D Torus topology to connect chips at the scale-up level to form a pod. The pod volume has increased to 9,600 cards (vs. 9216 cards for Ironwood), and the single-card scale-up bidirectional bandwidth is 19.2Tb (2x that of Ironwood), and we think that there are still 48 OCS in each pod, but the number of ports may increase to 300*300. To support the massive data requirements of TPU 8t, Google introduced Virgo Network for scale-out networking. This new networking architecture enables up to 4x increased data center network (DCN) bandwidth on TPU 8t training over DCN. Built on high-radix switches that reduce network layers by allowing more ports per switch, Virgo Network employs a flat, two-layer non-blocking topology. Compared with traditional datacenter networks, this significantly reduces latency by minimizing network tiers. It features a multi-planar design with independent control domains to connect TPU 8t chips. The TPU 8t racks also connect with the Jupiter north-south fabric to access compute and memory services. Virgo Network can connect more than 1 million TPU chips into a single training cluster, with a single network architecture connecting 134,000 chips.

Fig. 6: Virgo Network architecture



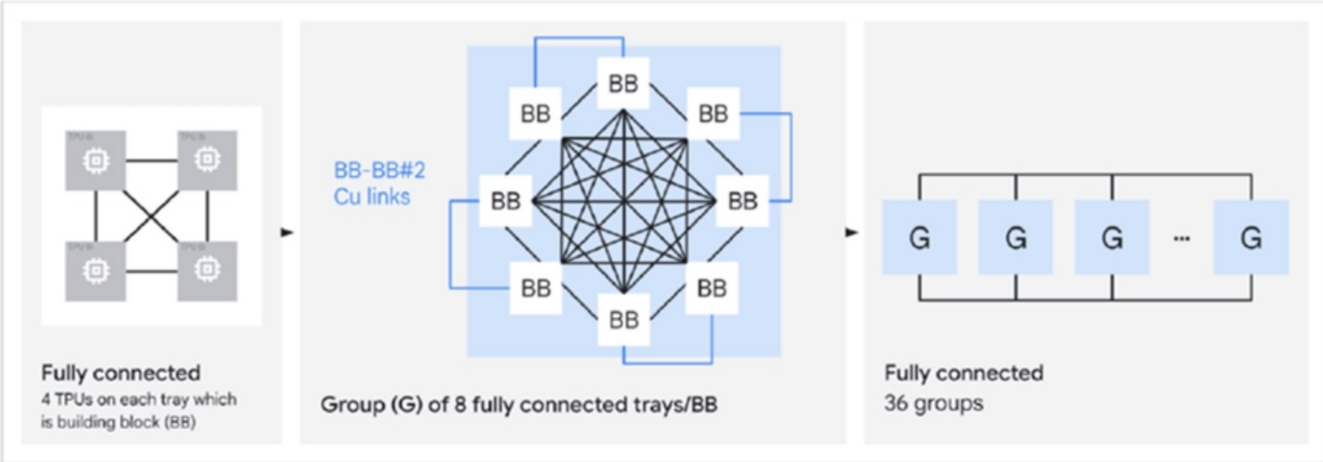
Source: Google, Nomura research

Google designed TPU 8i with a new serving optimized network topology called Boardfly. Boardfly is a flat two-layer architecture, significantly reducing the latency. Utilizing a high-radix design, Google connects up to 1,152 of these chips together, reducing the network diameter and the number of hops a data packet must take to cross the system. By slashing the hops required for all-to-all communication, Boardfly achieves up to a 50% improvement in latency for communication-intensive workloads, according to Google. For that same 1,024-chip pod, Boardfly reduces the network diameter from 16 hops down to 7, which directly leads to lower tail latency.

Boardfly consists of the following elements, and its topology is hierarchical by nature:

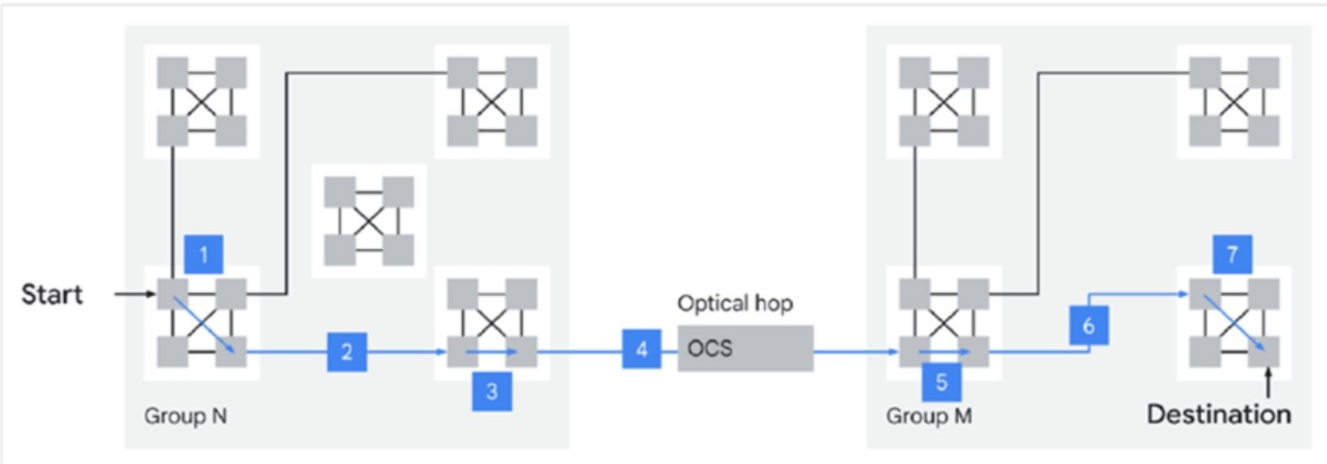
1. Building Block (BB): Each tray forms a **four-chip** ring using internal ICI links (**connected by PCB**), providing **16** external connections for broader networking.
2. Group (G): **8 boards** are fully connected via **copper cabling** to create a localized group, utilizing **11** of the available external links for intra-group communication.
3. Pod structure: The final architecture scales to **36 groups** (up to 1,024 active chips) linked through **Optical Circuit Switches (OCS),** ensuring a maximum latency of seven hops for any chip-to-chip communication.

Fig. 7: TPU 8i hierarchical Boardfly topology



Source: Google, Nomura research

Fig. 8: ICI network diameter via optical circuit switch on TPU 8i pod



Source: Google, Nomura research

Impact of TPU v8 on AI networking

The scale-up networking of TPU 8t continues the 3D Torus topology, and the pod volume has increased to 9,600 cards. The number of copper cables has also increased accordingly, while the optical transceiver ratio is about 1:1.5, according to Semi analysis, but the absolute number increases with the number of TPUs.

Fig. 9: TPU v7 3D Torus connection solutions

TPU v7 3D Torus Connection Solutions		
	Per TPU	Rack Total
8 Interior TPUs		
Copper cables	4	32
PCB Traces	2	16
Optical Transceivers	0	0
8 Corner TPUs		
Copper cables	1	8
PCB Traces	2	16
Optical Transceivers	3	24
24 Edge TPUs		
Copper cables	2	48
PCB Traces	2	48
Optical Transceivers	2	48
24 Face TPUs		
Copper cables	3	72
PCB Traces	2	48
Optical Transceivers	1	24
Total for 64 TPU Rack		
Copper cables	1.25	80
PCB Traces	1.00	64
Optical Transceivers	1.50	96

Source: SemiAnalysis, Nomura research

The design of Google TPU 8i shows that in addition to model training requiring high-density computing clusters, large-scale inference involving multi-agent collaboration and complex chain-of-thought is also communication-intensive, which increases the requirements for low latency between chips. Judging from Google's new Boardfly topology, copper cables are still the main interconnect method at the ICI level, and the demand for OCS extends from scale-out to scale-up between chipsets.

Fig. 10: Calculation of usage of DAC/optical transceiver/OCS in TPU 8i pod

	BB	Group	Between group
DAC	8x11x36=3168	-	-
Optical transceiver	-	5x8x36=1440	-
OCS	-	-	20 72*72 OCS / 5 288*288 OCS

Source: Nomura estimates

Theoretically, the switching response speed of scale-up networking for OCS is required to reach nanoseconds. The MEMS-based OCS relies on the mechanical motion of the micromirror and the DLC-based OCS relies on the rearrangement of liquid crystal molecules, both of which have a switching time in the millisecond range, which cannot meet this requirement in terms of physical principle. However, the SiPh-based OCS can achieve nanosecond-level switching by virtue of the principle of electronically controlled refractive index, which matches the requirements of the scale-up networking, but it is still in the small-batch delivery stage. As a representative manufacturer of SiPh-based OCS, iPronics (unlisted) has released a 32*32-port SiPh-based OCS in 2025 and expects to release a 64*64-port OCS in 2026. Meanwhile, it has cooperated with Fabrinet (FN US, Not rated) to build the world's first mass-produced SiPh-based OCS production line, which should enter operation from 2Q26, according to company. The new manufacturing line enables iPronics to scale production rapidly to meet customer demand for SiPh-based OCS in training and inference AI clusters. On the other hand, although MEMS-based OCS switching speed is relatively slow, Google has made up for its switching delay through software scheduling, which is also the current strategy adopted by Google. Therefore, we believe that both the solutions have the potential to be used in TPU v8 clusters, and we will continue to catch up the latest progress in SiPh-based OCS.

In addition, both the eighth-generation TPU chips are equipped with Google's self-developed ARM architecture Axion CPU as the main controller, which solves the host computing power bottleneck caused by data preprocessing delays. The number of CPUs has been upgraded from "1 CPU with 4 TPUs" to "1 CPU with 2 TPUs", and the number of CPU hosts per server has doubled. The CEO of Arm, Rene Haas, mentioned in latest earnings call that as AI shifts from "human-computer interaction" to "agentized continuous workloads", data center CPU capacity will more than quadruple and the market size will exceed USD100bn by 2030. We think that the rapid growth of demand for CPUs will drive revenue growth of CPU PCB suppliers, server foundries and other related supply chain manufacturers.

Google's TPU v8 series chips adopt a dual-vendor strategy, with the TPU 8t being co-designed by Google and Broadcom (AVGO US, Not rated), and the TPU 8i being designed by Google and MediaTek (2454 TT, Buy; covered by Aaron Jeng) for the first time. Broadcom has rich experience in high-performance ASIC design, and the pursuit of extreme computing performance and interconnect bandwidth in training chips is Broadcom's strength, while MediaTek has advantages in power efficiency and cost optimization. Compared to single-chip performance, inference chips need to provide higher inference throughput per-unit power consumption. MediaTek's low-power design experience in the mobile SoC market could be well used for the inference chip.

Based on Counterpoint Research's latest Global AI Server Compute ASIC Shipment Forecast, the combined TPU v8t and v8e shipments are projected to approach 5mn units in 2028, more than 10x growth from the ~400k units shipped in 2026. We believe that the separation of TPU v8 training and inference chips and strong demand will likely help further expand Google's TPU supply chain.

Fig. 11: Google PCB and CCL supply chain

Generation	Content	Time	Structure	CCL Material	CCL Supplier(s)	PCB Supplier(s)
TPU v6p	TPU UBB	2H25~	34L PCB (16+18, N+M)	M7, HVLP2	Panasonic, EMC	WUS, ISU, TTM, VGT
	CPU board **(New)**	4Q25~	22L PCB	M6	EMC, Panasonic	VGT, WUS, ISU, TTM, others?
TPU v7p, v7e	TPU UBB	mid-26~	36~40L+ PCB	M8+M6, HVLP3	Panasonic, EMC	WUS, ISU, TTM, LCS, VGT?
	CPU board (New)	4Q25~	22L PCB	M6	EMC, Panasonic	VGT, WUS, ISU, TTM, others?
	PCIe switch **(New)**	mid-26~	22-24L PCB	M8?	EMC	WUS, ISU, GCE, ZDT, others?
TPU v8t, v8i	TPU UBB? More other boards?	2028?	24~26L? **HDI?**	M8.5? M9Q?	Panasonic? EMC?	WUS, ISU, Unimicron, others?

Source: Nomura research

Fig. 12: OCS industry supply chain

MEMS				
Core components	MEMS array	Optical filter	Fiber collimator array	Lens array
Global supplier	Silex		Corning	
Domestic supplier	Yitoa Intelligent	Optowide Technologies, DOTI Micro	TFC, T&S, EverProX, Optowide Technologies	Focuslight Technologies
OCS manufacturer/foundry	Lumentum, Accelink, Eoptolink, Triple-stone, Calient, Advanced Fiber Resources (foundry), Taclink (foundry)			
DLC				
Core components	Liquid crystal light module	Fiber collimator array	YVO_4 crystal	
Global supplier	Coherent	Corning		
Domestic supplier		TFC, T&S, EverProX, Optowide Technologies	Castech, Optowide Technologies	
OCS manufacturer/foundry	Coherent, Celestica (foundry)			
DLBS				
Core components	Piezoelectric Ceramics module	Fiber collimator array		
Global supplier	Polatis	Corning		
Domestic supplier	Luster	TFC, T&S, EverProX, Optowide Technologies		
OCS manufacturer/foundry	Polatis, Luster			
SiPh-based solution				
Core components	SiPh chip	PIC	MPO	PCB
Global supplier	iPronic		Corning	
Domestic supplier			T&S, EverProX	
OCS manufacturer/foundry	iPronic, Taclink			

Source: Company data, Nomura research

Appendix A-1

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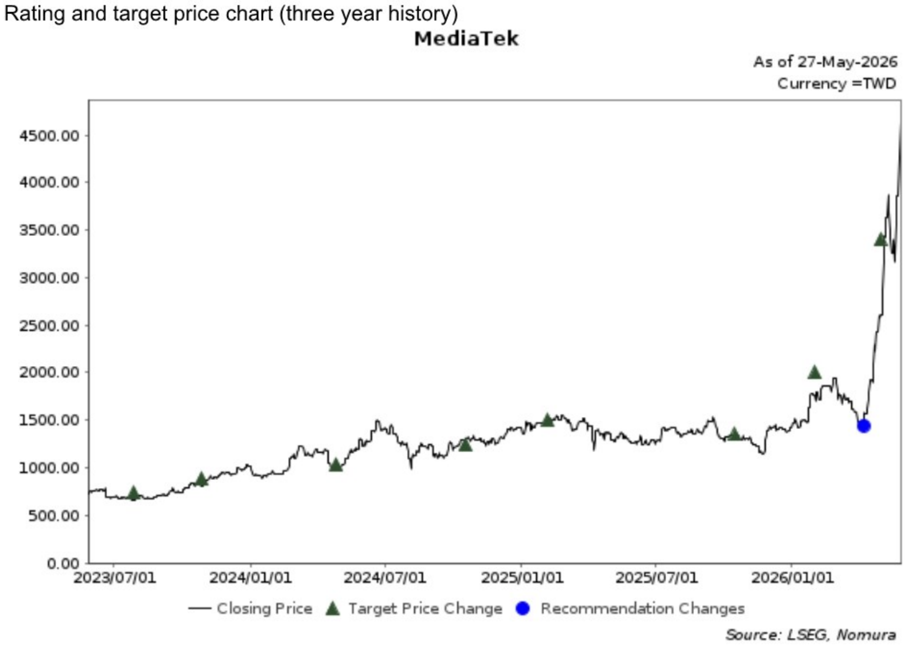
Materially mentioned issuers

Issuer	Ticker	Price	Price date	Stock rating	Sector rating	Disclosures
MediaTek	2454 TT	TWD 4,265.00	26-May-2026	Buy	N/A	
Victory Giant	2476 HK	HKD 436.80	27-May-2026	Buy	N/A	
Victory Giant	300476 CH	CNY 379.30	27-May-2026	Buy	N/A	

MediaTek (2454 TT) **TWD 4,265.00 (26-May-2026)** Buy (Sector rating: N/A)

Rating and target price chart (three year history)



Date	Rating	Target price	Closing price
30-Apr-26		3,400.00	2,610.00
30-Mar-26	Buy		1,510.00
01-Feb-26		2,000.00	1,760.00
16-Oct-25		1,350.00	1,330.00
05-Feb-25		1,500.00	1,525.00
17-Oct-24		1,250.00	1,275.00
26-Apr-24		1,040.00	1,005.00
27-Oct-23		890.00	801.00
28-Jul-23		740.00	658.00

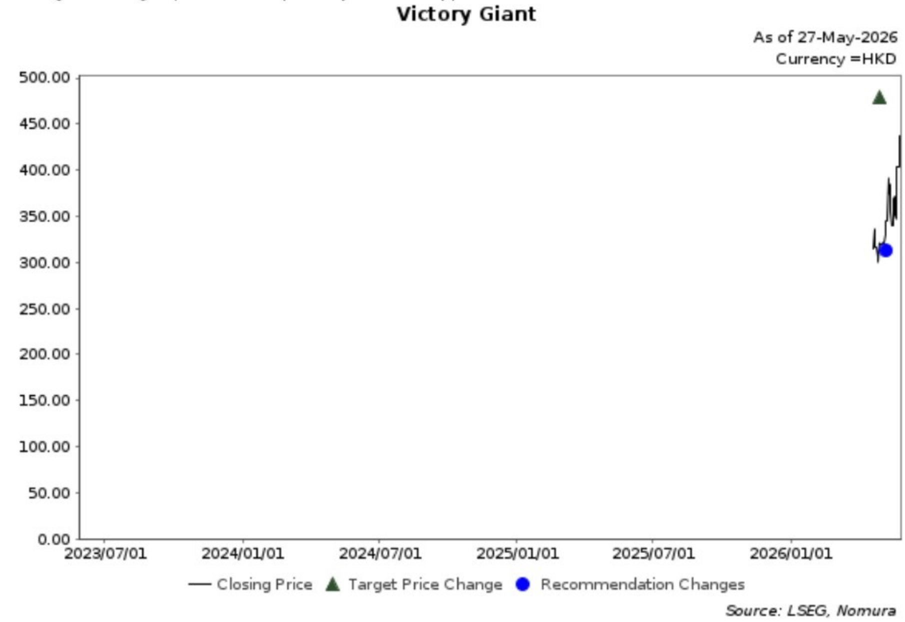
For explanation of ratings refer to the stock rating keys located after chart(s)

Valuation Methodology Our TP of TWD3,400 is based on 25x our average 2027-28F EPS. Our target multiple of 25x is at its high end of historical range. The benchmark index for this stock is TAIEX.

Risks that may impede the achievement of the target price Key downside risks include: 1) fierce price competition from Qualcomm and Spreadtrum; 2) the company's execution (i.e. a continuous rollout of good products in terms of specification, price and cost); 3) smartphone demand, especially in China and emerging markets, where MediaTek has higher revenue exposure; and 4) ASIC execution and competition.

Victory Giant (2476 HK) **HKD 436.80 (27-May-2026)** Buy (Sector rating: N/A)

Rating and target price chart (three year history)



Date	Rating	Target price	Closing price
30-Apr-26	Buy		319.40
30-Apr-26		479.00	319.40

For explanation of ratings refer to the stock rating keys located after chart(s)

Valuation Methodology Our TP of HKD479.00 is based on 27x 2027F EPS of CNY15.44, in line with its A-share historical median P/E. The benchmark index is Hang Seng Index.
Risks that may impede the achievement of the target price Downside risks: 1) lower-than-expected PCB demand in downstream sectors such as servers and auto electronics; 2) more fierce competition in the high-end PCB market leading to pressure on margins; 3) higher-than-expected raw material cost pressure, and 4) worse-than-expected geopolitical tensions in global AI value chain.

Victory Giant (300476 CH) **CNY 379.30 (27-May-2026)** Buy (Sector rating: N/A)

Rating and target price chart (three year history)

Date	Rating	Target price	Closing price
30-Apr-26		417.00	328.49
15-Jan-26		333.00	283.07
24-Oct-25	Buy		308.98
24-Oct-25		392.00	308.98

For explanation of ratings refer to the stock rating keys located after chart(s)

Valuation Methodology Our target price of CNY417.00 is based on 27x 2027F EPS of CNY15.44, in line with company's historical median P/E of 27x. The benchmark index is CSI300.
Risks that may impede the achievement of the target price Downside risks include: 1) key customers' supply chain diversification and more intensified competition from peers; 2) technology changes such as COWOP which may change the competition landscape and threat company's market shares; 3) slower technology upgrade in AI PCB market; and 4) escalations on geopolitical tensions.

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STOCKS

A rating of **'Buy'**, indicates that the analyst expects the stock to outperform the Benchmark over the next 12 months. A rating of **'Neutral'**, indicates that the analyst expects the stock to perform in line with the Benchmark over the next 12 months. A rating of **'Reduce'**, indicates that the analyst expects the stock to underperform the Benchmark over the next 12 months. A rating of **'Suspended'**, indicates that the rating, target price and estimates have been suspended temporarily to comply with applicable regulations and/or firm policies. Securities and/or companies that are labelled as **'Not rated'** or shown as **'No rating'** are not in regular research coverage. Investors should not expect continuing or additional information from Nomura relating to such securities and/or companies. Benchmarks are as follows: **United States/Europe/Asia ex-Japan:** please see valuation methodologies for explanations of relevant benchmarks for stocks, which can be accessed at: http://go.nomuranow.com/research/m/Disclosures; **Global Emerging Markets (ex-Asia):** MSCI Emerging Markets ex-Asia, unless otherwise stated in the valuation methodology; **Japan:** Russell/Nomura Large Cap.

SECTORS

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